45. (Twice Amended) The method of claim 44, wherein said depositing the insulating material comprises forming an oxide by a CVD method using the electrically inert source.

46. (Amended) The method of claim 36, wherein said insulating film is deposited directly on walls of the groove.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 9-11, 14-46, and 48-53 are pending in this application. Claims 16-23 have been withdrawn from consideration. Claim 47 was previously canceled without prejudice or disclaimer and Claims 9, 25-33, 36, 41, and 44-46 have been amended without the introduction of any new matter.

The outstanding Official Action presents an objection from the previous Office Action to Claims 28-33 and 46 under 35 U.S.C. § 132, a rejection from the previous Office Action of these claims under the first paragraph of 35 U.S.C. § 112 as including prohibited new matter, a rejection from the previous Office Action of Claims 9-11, 14, 15, 24-29, 34-45, and 49-53 under 35 U.S.C. § 103(a) as being unpatentable over Rogers et al, (U.S. patent No. 4,571,819, Rogers) in view of Lee et al (U.S. Patent No. 4,952,524, Lee), and a rejection from the previous Office Action of Claim 48 under 35 U.S.C. § 103(a) as being unpatentable over Rogers in view of Lee in further view of Hunter et al (U.S. Patent No. 4,631,803, Hunter). In addition, the outstanding Action presents a new objection to Claims 44 and 45 as well as a corresponding new rejection of Claims 44 and 45 under the second paragraph of 35 U.S.C. § 112, a new rejection of Claims 9-11, 14, 15, and 24-53 under the first paragraph of 35 U.S.C. § 112, a new rejection of Claims 9, 11, 14, 15, 24-41, 43-46, 49, 50, 51, and 53

under 35 U.S.C. § 103(a) as being unpatentable over Bose et al (U.S. Patent No. 5,492,858, Bose) in view of Anonymous RD 327019 (Anon '019), a rejection of Claims 10 and 42 over Bose in view of Anon '019 in further view of Rogers, and a rejection of Claims 48 and 52 under 35 U.S.C. § 103(a) as being unpatentable over Bose in view of Anon '019 in further view of alleged admitted prior art.

Turning first to the new objections and rejections raised as to Claims 44 and 45 based upon the recitation of an "insulating material" instead of an "insulating film," these objection and rejections are believed to be overcome by the present amendment to Claims 44 and 45 that substitute --film-- for "material."

Further as to the various old and new objections under 35 U.S.C. § 132 and corresponding rejections of various claims under the first paragraph of 35 U.S.C. § 112, the objections/rejections based upon the language "narrower than 0.5 μm" are now believed to be moot as this language has been deleted from Claims 9, 25, 26 and 27. Similarly, all objections and rejections based upon the previous recitation of "non doped" in Claims 9, 25-29, 36, and 45 are now believed to be moot as this language has been deleted from these claims.

In addition the objections and rejections under 35 U.S.C. § 132 and the first paragraph of 35 U.S.C. § 112 are traversed as to the noted claim language of "depositing oxide film directly on the thermal oxidation film" (in Claims 28 and 29) and the modification to Claims 30-33 and 46 that modify these claims to now recite the "oxide films" as either deposited or buried "directly on walls of the groove."

In this regard and as noted in the response filed January 18, 2002:

> Besides the fact that the objection under 35 U.S.C. §132 to Claims 28-33 and 46 violates the PTO's own guidelines, it is further clearly without merit for the reasons presented below as to traversing the corresponding rejection of Claims 28-33 and 46 under the first paragraph of 35 U.S.C. §112.

In this regard, the outstanding Office Action appears to have committed further error in basing this rejection on the exact claim language not appearing in the specification as filed with respect to the language added by the amendment to these claims made on June 13, 2001, that states that the "oxide films are deposited [as in Claims 31 and 46, or "buried" as in Claims 32 and 33] in the grooves so as not to include any nitride film in the grooves" or the requirement for "depositing oxide film directly on the thin thermal oxidation films" set forth by Claims 28 and 29. However, as further explained in the PTO's own guidelines of MPEP §2163 (at page 2100-161 of August 2001 revision):

> An applicant may show possession of an invention by disclosure of drawings or structural chemical formulas that are sufficiently detailed to show that applicant had possession of the claimed invention as a whole. See, e.g., *Vas-Cath*, 935F.2d at 1565, 19 USPQ2d at 118 ("drawings alone may provide a "written description" of an invention as required by Sec. 112\"); *In re Wolfensperger*, 302 F.2d 950, 133 USPQ 537 (CCPA1962) ("the drawings of applicant's specification provide sufficient written descriptive support for the claimed invention at issue); *Autogiro Co. Of America v. United States*, 384 F.2d 391, 398, 155 USPQ 697, 703 (Ct. Cl. (1967) ("In those instances where a visual representation can flesh out words, drawings may be used in the same manner and with the same limitations as the specification.") ... .

Thus, the present rejection of Claims 28-33 and 46 under the first paragraph of 35 U.S.C. §112 is in error in that it ignores the clear written descriptive support that is present in the showings of Figs. 3A-E, for example, with respect to the language added by the amendment made on June 13, 2001, requiring that "oxide films are deposited [as in Claims 31 and 46, or "buried" as in Claims 32 and 33] in the grooves so as not to include any nitride film in the grooves" or the requirement for "depositing oxide film directly on the thin thermal oxidation films" set forth by Claims 28 and 29. In this respect, the absence of "any nitride film in the grooves" and the fact that the illustrated oxide film "is directly on the thin thermal oxidation films" could not be any clearer.

> Besides improperly ignoring Figs.3A-E, for example, the outstanding Office Action ignores the specification description of the deposit of the oxide films 71 in the groove 6 at page 6, lines 3-15, for example. Moreover, even though the Examiner notes that page 19, line 26 suggests that a Si_3N_4 layer may be grown, the fact that a substitute thermal oxidation film can be used or that both of these alternatives can be omitted under the teachings of the paragraph beginning at line 22 of page 19 has been erroneously ignored. In this regard, "may" is not a synonym for "must," it is a permissive term well

understood to only indicate possibilities, not absolutes. Thus, Page 19, lines 24-26, instruct the artisan that omit both the thin thermal oxidation film and the Si3N4 film can be omitted as part of the invention, not that either or both must be included. This is particularly true in light of Figs. 3A-3E that show the case where an oxide film is directly deposited on the inner wall of the groove. Accordingly, as there is clear support in the application as filed, the rejection of Claims 28, 29, 30-33 and 46 under the first paragraph of 35 U.S.C. §112 is traversed as these claims are clearly directed to one of the optional choices available as described in the application..

This last point was again emphasized at the discussion held with the Examiner on October 18, 2002 by pointing out that the that the alternatives taught at page 19, lines 24-26, teach different embodiments in which either or both the thin thermal oxidation film and the Si3N4 film can be omitted as part of the invention, and that there is no prohibition as to claiming any alternative embodiment reasonably disclosed as such. If the objection and rejections are repeated, the authority for ignoring the case law, the MPEP, and the clear statements of the specification as well as the drawings is respectfully requested.

In addition, Applicants note that the limitation of "non doped" in Claims 9, 25-29, 36, and 45 has been changed to --electrically inert-- by the present amendment. It is clear that the language --electrically inert-- means that the organic silicon source cannot contain well known electrically active impurity elements, such as boron, phosphorus, and arsenic. This prohibition as to containing any electrically active impurity elements clearly prohibits the use of any well known electrically active organic silicon source, such as borosilicate glass (BSG), phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG), that contain such well known electrically active impurity elements. This limitation as to an "electrically inert" organic silicon source allows for the presence of known electrically inactive elements, such as oxidizing agent in the organic silicon source, a noted on page 19, lines 30-36 of the

specification. In this regard, it is well known that an oxidizing agent, such as N_2O, O_2, or O_3, does not serve as an electrically active element acting as a donor or acceptor.

Fig. 7B of this application clearly shows the relationships between the etching rates of the "electrically inert" oxide film and annealing temperature. If the oxide films are doped with "electrically active" elements, such as boron or phosphorus, the relationships between the etching rates and annealing temperature would be different.

Furthermore, the respective Raman intensities measured in the wave number region ranging from 300 cm^{-1} to 700 cm^{-1} as shown in Figs. 6A and 6B of the original disclosure of this application clearly represent the Raman spectra of an "electrically inert" silicon oxide film deposited by CVD using an "electrically insert" organic silicon source. In this regard, if the silicon oxide film contained "electrically active" elements, such as boron, the Raman spectra would reveal them. Note, for example, the peak at 670 cm^{-1} in Fig. 3 and table 3 of attached reference. Similarly if the silicon oxide film contains "electrically active" phosphorus, the Raman spectra has a peak at 520 cm^{-1} as shown by Fig. 4 and table 4 of the same attached reference. As there is no peak at 670 cm^{-1} or 520 cm^{-1} or elsewhere that indicates the presence of an electrically active element in the silicon oxide films relative to the Raman spectra shown in Figs. 6A and 6B of the original disclosure, it can be concluded that the Raman spectra shown in Figs. 6A and 6B demonstrate that there are no such electrically active elements present.

Furthermore, it is well recognized in the art that if TEOS contains "electrically active" element, such as boron or phosphorus, it is labeled with an appropriate acronym such as "BPTEOS" or "doped TEOS," that clearly distinguishes it from ordinary "TEOS." Note, for example, column 4, lines 31-38 of the above noted relied upon Lee reference. That is,

workers in the art understand that use of the term "TEOS" alone means that there are no "electrically active" elements included.

As it is well established that an inherent property of a disclosed embodiment can be claimed as if that inherent property were actually set forth in the original specification, the claiming here of the inherent "electrically inert" nature of the organic silicon source is not new matter. See MPEP § 2163.07(a) and the case law cited therein.

In addition to the above, it was pointed out to the Examiner during the above-noted discussion that the repeated obviousness rejections from the prior Office Action were all in error in that they were clearly based on ignoring the limitation that were rejected under the first paragraph of 35 U.S.C. § 112 and/or objected to under 35 U.S.C. § 132. This "error" has been stated by the U.S. PTO Board of Patent Appeals and Interferences in Ex parte Gasselli, 231 USPQ 393, 394 (1983) aff'd mem. 783 F.2d 453 (Fed. Cir. 1984) as follows:

> We also note that many of the remaining references required the presence of other elements expressly excluded from the present claims, i.e., halogen, uranium or the co-presence of vanadium and phosphorus. All of these limitations of the claims must be considered regardless of whether or not they were supported by the specification as filed. *In re Wilson*, 57 CCPA 1029, 424 F.2d 1382, 165 USPQ 494 (1970); *In re Miller*, 58 CCPA 1182, 441 F.2d 689, 169 USPQ 597 (1971).

Accordingly, the rejection of Claims 9-11, 14, 15, 24-29, 34-45, and 49-53 under 35 U.S.C. § 103(a) as being unpatentable over Rogers in view of Lee and the rejection of Claims 47 and 48 under 35 U.S.C. § 103(a) as being unpatentable over Rogers in view of Lee in further view of Hunter from the last action are traversed as being made based upon erroneously ignoring claim limitations and the arguments repeated from the above-noted previous response and are traversed for this reason. If these rejections are again repeated an appropriate explanation as to how the relied upon references are being interpreted to meet all of the limitations of these claims is believed to be appropriate.

Turning to the newly presented obviousness rejections applied as to Claims 9- 11, 14, 15, 24-46, and 48-53, it is clear that the outstanding Action misinterprets the teachings of Bose as to the required presence of the nitride layer that is needed to allow densification of the deposited dielectric material as explained at col. 4, lines 1-12 thereof. Accordingly, their has been no establishment of a prima facie case of obviousness as to the subject matter of Claims 28-33.

Furthermore, the reliance on Anon '019 as to reducing stress in some manner that could be used to supplement or reasonably modify the teachings of Bose is further clearly misplaced as being based upon an improper analysis of what these references actually teach.

In this regard, it is clear that Anon '019 discloses using TEOS/O_3/O_2 as a source gas in thermal CVD to deposit film having a thickness of 300-400 nm, then annealing in an ambient of Ar or N_2, O_2, at a temperature range of 800-1150 degrees C for only 30 seconds. Thus, in Anon '019 there is no disclosure or suggestion of claimed annealing temperature range of 1150-1350 degrees C, although the lower boundary temperature of 1150 degrees C is taught. Missing from the analysis in the outstanding Action, however, is the required showing of motivation to select just the upper limit temperature of 1150 degrees C from the Anon '019 taught range of temperatures for rapid annealing when this temperature exceeds the 1100 degrees C upper limit noted by Bose while there are other temperatures in the Anon '019 suggested temperature range (800-1150 degrees C) that correspond to the temperatures used by Bose. The need for specificity as to establishing motivation was set forth in In re Lee, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) as follows:

> The need for specificity pervades this authority. See, e.g., In re Kotzab, 217 F. 3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); In re Rouffet, 149 F. 3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the

art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1250, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

* * *

This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983), Thus, the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion.

Furthermore, the outstanding Action ignores that the steam atmosphere annealing step of Bose is to be performed for "about 60 to 90 minutes" as explained at col. 5, lines 56-59. Is the outstanding Action suggesting that the artisan would reduce this time to 30 seconds and use the annealing ambient taught by Anon '019 even though the teaching of Bose is to steam anneal for the 60 to 90 minutes, as noted above, and even though the artisan would have realized that both the annealing time and the annealing temperature must be simultaneously considered in terms of their combined effect on the thermal process and resulting thermal phenomena? Clearly, given the totally different ambient conditions and annealing times required by Bose, it would not even have occurred to the artisan to attempt to combine the disparate teachings of these references because to do so means that neither one would function as intended which is the exact opposite of a showing of reasonable motivation. See In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984). Thus, the artisan would have understood

that the proposed combination of Bose and Anon '019 would be impossible as they are concerned with entirely different types of annealing.

To the extent that the outstanding Action attempts to suggest that a valid *prima facie* case of obviousness can be established by merely citing individual references teaching that individual ones of the claim limitations were "known," this approach is clearly in error. As recently noted by the court in In re Kotzab, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000):

> Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. *See id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See id.* Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. *See In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

Furthermore, Anon '019 is silent about any cause-effect relationship between stress and dislocation defects and does not teach or suggest the claimed "dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}" or any other dislocation density. Thus, even though Anon '019 notes that "stress reduction results," Anon '019 fails to show the stress reduction results in the claimed "dislocation density." Anon '019 is further silent about stress generated in the substrate, and merely state that "thick films of 1.26 micron can be deposited without defects or cracking." It is evident that the position of the defect generation of concern is in the oxide film in Anon '019, not in "the corresponding device region in a vicinity of the grooves" as claimed.

Thus, with respect to Claims 9 and 25, the apparent belief that following the time and temperature teachings of Anon '019 guarantees that the dislocation density generated in the corresponding device region in a vicinity of the grooves is inherently less than 1 μm^{-2} is not

well founded any more than the apparent belief that there would be some reason to use the temperature of 1150 degrees C with Bose is based on the teachings of these references. In this regard, it is well established that inherency requires the certainty that something will happen, not merely a possibility or even a probability that something may occur. See In re Robertson, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) and In re Oelrich, 212 USPQ 323, 326 (CCPA 1981).

With respect to Claims 26 and 27, the outstanding Action incorrectly asserts that the 4-fold or 5-fold ring structure of the oxide film is the inherent result of annealing the oxide film at a high temperature as taught by Anon '019. However, as explained above, a thermal process result does not simply depend on the temperature applied because the time it is applied for is also critical to the result achieved. Here, it is clear that the claimed 4-fold or 5-fold ring structure of the oxide film cannot obtained at the lower temperature range of 800-1150 degrees C which is applied for the 30 seconds suggested by Anon '019, even if the 1150 degrees C temperature is arbitrarily selected. This is because TEOS contains carbon (C) as a principal component and it is well known that carbon (C) is hard to evaporate from the TEOS with the lower temperature range of Anon '019 applied for only 30 seconds. Clearly, there is no logical basis to assume inherency in view of the vastly different annealing condition as between Anon '019 and those disclosed as necessary to achieve the claimed ring structure of the oxide film.

Accordingly, the rejection of Claims 9, 11, 14, 154, 24-42, 43-46, 49, 50, 51 and 53 under 35 U.S.C. § 103 over Bose in view of Anon '019 is also traversed.

Furthermore, as Rogers and the alleged prior art relied on to additionally reject Claims 10, 42, 48 and 52 cure none of the deficiencies noted above as to Bose and Anon '019, these rejections are traversed for the above noted reasons. In addition, each of these

rejections rely on mere knowledge which is not reliance on proper motivation to establish a *prima facie* case of obviousness and are traversed for that reason as well. Note the above quoted language from In re Kotzab.

As no further issues are believed to remain outstanding in this application, it is believed that this application is clearly in a condition for formal allowance and an early and favorable action to this effect is, therefore, respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

Please amend Claims 9, 25-33, 36, 41, and 44-46 as follows:

--9. (Five times amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and a device region sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate[, each of grooves having a width narrower than 0.5μm];

(b) depositing oxide films in the grooves by a CVD method using [a non doped] an electrically inert organic silicon source;

(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

25. (Four times amended) A method of manufacturing a semiconductor substrate having [a] shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate[, each of grooves having a width narrower than 0.5μm];

(b) depositing oxide films in the grooves by a CVD method using [a non doped] an electrically inert organic silicon source;

(c) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so the dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(d) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

26. (Four times amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate[, each of grooves having a width narrower than 0.5μm];

(b) burying oxide films in the grooves by a CVD method using [a non doped] an electrically inert organic silicon source; and

(c) annealing said oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, and an etching rate by ammonium fluoride solution of said oxide films is less than 130 nm/min, which is substantially identical to that of a thermal oxide film.

27. (Four times amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate[, each of grooves having a width narrower than 0.5μm];

(b) burying oxide films in the grooves by a CVD method using [a non doped] an electrically inert organic silicon source; and

(c) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C, but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective ring structures to a total integrated Raman intensity, and the structures are formed to satisfy either of or both conditions that said higher order ring structures are substantially more than 85 % of an overall structure and said lower order ring structures are substantially less than 15 % of the overall structure.

28. (Four times amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by a CVD method using [a non doped] an electrically inert organic silicon source;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(e) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

29. (Four times amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by a CVD method using [a non doped] an electrically inert organic silicon source;

(d) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(e) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

30. (Amended) The method of claim 9, wherein said oxide films are deposited directly on walls of the grooves [so as not include any nitride film in the grooves].

31. (Amended) The method of claim 25, wherein said oxide films are deposited directly on walls of the grooves [so as not include any nitride film in the grooves].

32. (Amended) The method of claim 26, wherein said oxide films are buried directly on walls of the grooves [so as not include any nitride film in the grooves].

33. (Amended) The method of claim 27, wherein said oxide films are buried directly on walls of the grooves [so as not include any nitride film in the grooves].

36. (Twice Amended) A method for forming a microelectronic structure, the method comprising:

(a) forming a mask layer on a substrate wherein the mask layer exposes a part of the substrate;

(b) forming a groove in the exposed part of the substrate

(c) depositing a layer of an insulating film using [a non doped] an electrically inert source so as to fill the groove and cover the mask layer;

(d) annealing said insulating film at a temperature which is greater than or equal to 1150°C but less than or equal to 1350°C.

41. (Amended) The method of claim 36, further comprising:

planarizing said insulating [material] film so that the substrate is exposed.

44. (Amended) The method of claim 36, wherein said forming the layer of the insulating [material] film comprises forming an oxide layer on inner walls of the groove and depositing an insulating material on the oxide layer to fill the groove.

45. (Twice Amended) The method of claim 44, wherein said depositing the insulating material comprises forming an oxide by a CVD method using the [non doped] electrically inert source.

46. (Amended) The method of claim 36, wherein said insulating film is deposited directly on walls of the groove [so as not include any nitride film in the groove].--